Amendments to the Drawings:

The attached replacement drawing sheet includes amendments to the drawing version of Figure 4 submitted in the January 25, 2005 Amendment. The replacement sheet replaces the previously submitted sheet numbered 3/5. In the corrected drawing, reference numerals "405.1-405.8" are used (as in the originally-filed drawings), rather than the reference numerals "5.1-5.8", which were mistakenly used in the drawing version of Figure 4 submitted in the January 25, 2005 Amendment. Additionally, the "ALIAS" signal applied to the "Decision Logic" block 411 in Figure 4 has been corrected. The reference numeral amendments and the amendment to the "ALIAS" signal are both in agreement with and consistent with the originally filed patent application. Further, no new matter is entered by the drawing changes. In addition to the replacement sheet, an annotated sheet showing changes in red is attached to this Amendment.

Attachments: Replacement Sheet
Annotated Sheet Showing Changes

REMARKS

Claims 1-9 are pending in the subject patent application. Claims 1, 5, 8 and 9 have been amended. Applicant respectfully requests consideration of the claims in view of the amendments made herein and the remarks provided below.

Objections to the Drawings

In the May 27, 2005 Office Action, the drawings were objected to for failing to comply with 37 C.F.R. § 1.84(p)(5) for having incorrect reference numerals and for mistakenly showing the "ALIAS" signal as being an output of the summation block 409 in Figure 4 of the drawings. In response, Applicant has amended the Figure 4 of the drawings to correct the mistakes. Applicant requests, therefore, that the drawing objections be withdrawn.

Claim Objections – Claim 1 and 9

In the Office Action, Claim 1 was objected to for using "second intermediate values" rather than recommended "second intermediate **value**" in line 11 of the claim. Claim 9 was objected to for using "values" instead of the recommended "value". For the following reasons, Applicant respectfully disagrees with these objections.

Regarding the objection made to Claim 1, Applicant disagrees that "second intermediate values" should be amended to read "second intermediate **value**". Claim 1 recites that "each delayed version of the derived clock signal" is sampled "at successive times defined by the known clock signal to produce first intermediate values". Claim 1

further recites that "transition detection using the first intermediate values" is employed to "produce second intermediate values". From a claims construction standpoint, while it is possible that, "for each delayed version of the derived clock signal" only a single, "second intermediate value" is generated per clock period of the known clock (e.g., as described in the preferred embodiments), the Claim 1 is not restricted to a single cycle of the known clock signal. For example, multiple "second intermediate values" may be produced over multiple clock cycles of the known clock signal and the claims is still clear and definite. Accordingly, Applicant respectfully believes that the objection to Claim 1 for using the term "second intermediate values" (rather than the suggested "second intermediate value") cannot be properly maintained and requests that it be withdrawn.

Claim 9 was also objected to for using "values" rather than "value". While Applicant disagrees that the word "values" renders the claim indefinite, Claim 9 has been amended in this amendment to claim an embodiment of the invention where "each chain" of "a first logic section including multiple chains of flip flops" produces an "intermediate value for each period of the known clock signal". Because the objected to "values" is no longer being present in Claim 9, Applicant requests that the objection to Claim 9 for use of the word "values" be withdrawn.

Claim Rejections – 35 U.S.C. § 112, Second Paragraph -- Claims 1-9

In the Office Action, Claims 1-9 were rejected under 35 U.S.C. § 112, second paragraph for allegedly being indefinite.

In particular, Claim 1-7 were rejected for allegedly including unclear language in Claim 1, lines 4-6 and Claim 5, lines 4-7. With respect to Claim 1, the Examiner asks "is the derived clock signal provided to the input of the first delay element in a series of delay elements to form the multiple delayed versions of the derived clock signal"? Or is the derived clock signal provided simultaneously to multiple delay elements?" Claim 1 clearly recites a step of "forming a sequence of multiple delayed versions of the derived clock signal". Applicant respectfully believes that there is nothing unclear with use of this language. Ostensibly, the Examiner is asserting that the claim is unclear for not including in the claim the apparatus used to perform the step. However, there is no rule requiring the step of a method claim to specify what apparatus the step uses to perform the recited function.

Claim 5, although it is an apparatus claim, clearly recites that a "delay chain of logic elements, coupled to the derived clock signal and the unknown clock signal" is what is employed to "form a sequence of multiple delayed versions of the derived clock signal". Applicant respectfully believes that this claim language is definite and not confusing. Further, Applicant respectfully disagrees that the claim language "each delayed version following a first delayed version in the sequence being delayed more than a previous delayed version in the sequence" is indefinite or in any way confusing. Clearly, such claim language describes how at least two of the "multiple delayed versions" are delayed relative to the another. There is nothing unclear or indefinite about the language.

Claims 5-7 were also rejected as being indefinite, for not specifying in Claim 5 whether the word "each" in line 8 is referring to each of the sample chains or each of the logic elements"? In response, Applicant has amended Claim 5 so that it is clear that the word "each" in line 8 of Claim 5 refers to "each sampling chain". In light of the amendment, Application respectfully requests that the indefiniteness rejections of Claims 5-7 be withdrawn.

Claims 8 and 9 were rejected as being indefinite, for not clearly specifying whether the formed number stream represents the frequency/phase of the known clock signal or the frequency/phase of the unknown clock signal. In response, Applicant has amended Claim 8 so that it is clear that "said number stream represent[s] the frequency or phase of the unknown clock signal". Claim 9 has also been amended to avoid any ambiguity. In light of the amendments, Application respectfully requests that the indefiniteness rejections of Claims 8 and 9 be withdrawn.

Claim Rejections – 35 U.S.C. § 102, Claims 1, 2 and 5

In the Office Action, Claims 1, 2 and 5 were rejected under 35 U.S.C. § 102(b) for allegedly being anticipated by U.S. Patent No. 5,892,384 to Yamada et al. For the following reasons Applicant respectfully disagrees.

Yamada et al. discloses a timing signal generator that is configured to receive an external clock signal and generate a pseudo-negative delay. An external clock signal input 1 is configured to receive the external clock signal, and a signal output terminal is configured to provide the timing signal having the pseudo-negative delay. An offset

delay circuit 2 and a detection delay circuit 3 having a plurality of intermediate taps are coupled to the external clock signal input terminal 1 via a waveform reform circuit. A sample/hold circuit 4 is connected to each intermediate tap of the detection delay circuit 3. A sampling signal is simultaneously provided to the sample/hold circuits 4, so that the sample/hold circuits 4 sample and hold voltages taken at the respective intermediate taps of the detection delay circuit 3 at a given moment. The signal levels of the respective intermediate taps at the moment of inputting the sampling signal to the sample/hold circuits 4 are sampled by the corresponding sample/hold circuits 4 and input to the respective corresponding boundary detection circuits 5.

Yamada et al. is distinguishable from independent Claim 1 of the present application in various respects. First, Claim 1 claims a method of "sampling an unknown clock signal", while Yamada et al. is directed at generating a signal having a pseudo negative delay from an external clock signal. There is nothing in Yamada et al. indicating that the "external clock signal" is an unknown clock signal. Accordingly, the first step in the method of Claim 1 (i.e., "forming from [an] unknown clock signal a derived clock signal") is not taught by Yamada et al. Further, Yamada et al. fails to teach "combining the second intermediate values produced from the delayed versions of the derive clock signal to produce sample values." Despite what is asserted in the Office Action, the "output selection circuit 6" in Figure 2 of Yamada et al. is not a combining circuit. Further, the output selection circuit 6 of Yamada et al. does not combine "second intermediate values produced from the delayed versions of a clock derived from an unknown clock signal "to produce sample values". Rather, the output of the timing

signal generation circuit of Yamada et al. is a signal extracted from one of the taps depending on the signals applied to the output selection circuit 6. Accordingly, for at least these reasons, Yamada et al. does not anticipate independent Claim 1 of the present application. Claim 2 depends from independent Claim 1 and, therefore, derives patentability for at least the same reasons independent Claim 1 does.

Claim 5 was also rejected for allegedly being anticipated by Yamada et al. Comparing Claim 5 to Yamada et al. reveals the following important distinctions. First, there is nothing in Yamada et al. indicating that the external clock signal is an "unknown clock signal". Further, Yamada et al. fails to teach "multiple sampling chains of logic elements", where "each sampling chain is coupled to one of...multiple delayed versions of the derived clock signal and to the known clock signal." The sample and hold circuits 4 are not "sampling chains of logic elements". Even if they could be so characterized, they are not coupled to *both* "one of the multiple delayed versions of the derived clock signal and the known clock signal". Indeed the sample and hold circuits 4 are coupled to what appears to be a known clock signal (i.e. the external clock signal) and to a delayed version of the external clock signal (i.e., to the output signal produced from delay circuit 2). Finally, Yamada et al. fails to teach a "combining circuit" that "logically combin[es] output signals of...transition detection circuits". As explained above in response to the rejection of independent Claim 1, the output selection circuit 8 is not a "combining circuit". For at least the foregoing reasons, Applicant respectfully believes that the § 102 rejection of independent Claim 5 cannot be properly maintained. Applicant requests, therefore, that the rejection be withdrawn.

Claim Rejections – 35 U.S.C. § 102, Claims 8 and 9

In the Office Action Claims 8 and 9 were rejected for allegedly being anticipated by U.S. Patent No. 6,606,004 to Staszewski et al. For the following reasons, Applicant respectfully disagrees.

Staszewski et al. discloses an apparatus and technique for time dithering a digitally controlled oscillator. The apparatus employs a shift register, a multiplexer, and a sigma-delta modulated delay control. As explained in column 12, line 67 through column 13, line 4, the sigma-delta modulator randomizes the small discrete timing deviations to the actual repetitive update of the digitally controlled oscillator (DCO) 200 such that the compare-frequency spurs are sufficiently blurred in to the background noise.

In the Office Action, it is asserted that the signal from the sigma-delta modulator that is applied to the multiplexer in Figure 15 of Staszewski et al. is an "alias value", as that term is used in independent Claim 8 of the present application. Applicant respectfully disagrees. The "alias value" in Claim 8 is recited to have a value that "indicat[es] an expected frequency range of a received unknown clock signal." Not only does Staszewski et al. fail to teach receiving an "unknown clock signal" (the reference signal 1500 is a known clock signal), it also fails to teach "applying...an alias value indicating an expected frequency range of a received unknown clock signal." The signal from the sigma-delta modulator in Figure 15 of Staszewski et al. does not indicate "an expected frequency range of a received unknown signal." For at least the foregoing reasons, Staszewski et al. does not anticipate independent Claim 8 of the present

application. Applicant requests, therefore, that the § 102 rejection of independent Claim 8, as allegedly being anticipated by Staszewski et al., be withdrawn.

Similar reasons as to why independent Claim 8 is distinguishable over Staszewski et al. apply to the rejection of independent Claim 9. Specifically, Staszewski et al. fails to teach a "second logic section configured to receive an alias value indicating an expected frequency range of an unknown clock signal." Staszewski et al. also fails to teach a "second logic section" that is "operable to compare the alias value to sums of the intermediate values produces by said multiple chain of flip-flops to form [a] number stream." The multiplexer in Figure 15 of Staszewski et al. does not compare data at its inputs to an alias value. Indeed the multiplexer performs no comparing function whatsoever. Accordingly, for at least the foregoing reasons, the § 102 rejection of independent Claim 9, as allegedly being anticipated by Staszewski et al., cannot be properly maintained. Applicant requests, therefore, that the rejection be withdrawn.

Claim Rejections – 35 U.S.C. § 103(a), Claims 1 and 5

In the Office Action, Claims 1 and 5 were rejected for allegedly being unpatentable over U.S. Patent No. 5,528,637 to Sevenhans et al. For the following reasons, Applicant respectfully disagrees.

Sevenhans et al. discloses a synchronizing circuit (SC) that recovers from input data (ID) applied thereto a data clock signal (DC) synchronous therewith in frequency and in phase. The SC includes a tuned tapped delay line (TDL) that generates a plurality of mutually delayed clock signals (DCS) from a local clock signal (LCS). The delayed

clock signals (DCS) are applied to both a sampling circuit means (SM), which latches the sampled versions of the delayed local clock signals, and to inputs of comparators C1-C4. The sampling circuit (SM) is controlled by the input data (ID), which has a bitrate of 622 Mbit/s and is synchronous with a serial transmit clock frequency of 620 MHz, and samples and latches the actual values of the delayed clock signals (DCS) at the occurrence of input data level transitions. The sampling circuit means (SM) further provides on its outputs sampled and latched delayed clock signal values (LCSV), which are applied to second inputs of the comparators C1-C4. Each of the comparators C1-C4 pairwise compares the delayed clock signals (DCS) with respective ones of the sampled clock signals (LCSV). The outputs of the comparators C1-C4 are connected via a wire-OR connection, thereby allowing the generation of the data clock signal on the line DC synchronous with the input data on the input data (ID) line. The data clock signal is used to clock four latch circuits L1-L4, which are coupled in series so as to constitute a shift register. By the synchronous data clock signal DC, the input data is thus sampled and shifted in successive ones of the latch circuits L1-L4. Finally, the data clock signal is further divided by four (by a divide-by-four circuit, (DIV)), thereby providing at its output a 155 MHz clock signal, which is synchronous with the signal on the data clock (DC) line.

Comparing Sevenhans et al. to independent Claim 1 of the present invention reveals the following important distinctions. First, Sevenhans et al. does not teach or suggest "forming from [an] unknown clock signal a derived clock signal." Despite what is asserted in the Office Action, the TDL does not perform such an operation. The local

clock signal (LCS) applied to the TDL is a known clock signal having a known frequency. Hence, the first step in Claim 1 is not taught or suggested by Sevenhans et al. Because Sevenhans et al. fails to teach or suggest forming a "derived clock signal" from "an unknown clock signal", the remaining steps in Claim 1, which rely on such a formation, are not taught or suggested by Sevenhans et al. For example, because Sevenhans et al. fails to teach or suggest forming a "derived clock signal" from "an unknown clock signal", the subsequent step of a "forming sequence of multiple delayed versions of the derived clock signal..." is not taught or suggested by Sevenhans et al. Similar distinctions apply with respect to the rejection of independent Claim 5.

Moreover, because the Sevenhans et al. invention is a clock recovery circuit, which uses known characteristics (e.g. data rate) of received input data to recover a clock signal from the data, the input data signal is always a required input of the Sevenhans et al. apparatus. Despite this, in the Office Action it is asserted that the input data (ID) in Sevenhans et al. apparatus could be modified to use a clock signal (rather than an input data signal) "in order to synchronize a received clock with a local clock." Applicant respectfully disagrees with this proposed modification, since the proposed modification would both change the principle of operation and render the Sevenhans et al. apparatus unsatisfactory for its intended purpose – both of which are prohibited in making an obviousness rejection. *See* M.P.E.P. § 2143.01.

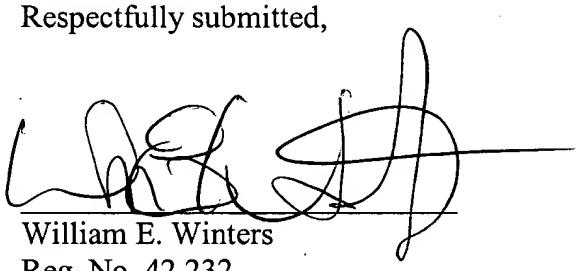
For at least the foregoing reasons, Applicant respectfully believes that the § 103 rejections of Claim 1 and 5, as allegedly being obvious over Sevenhans et al., cannot be properly maintained. Applicant requests, therefore, that the rejections be withdrawn.

CONCLUSION

For at least the foregoing reasons, Applicant believes all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner has any further questions or comments concerning the amendments made herein, he is encouraged to telephone the undersigned at 408-282-1857.

Respectfully submitted,



Dated: AUGUST 29, 2005

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Annotated Sheet

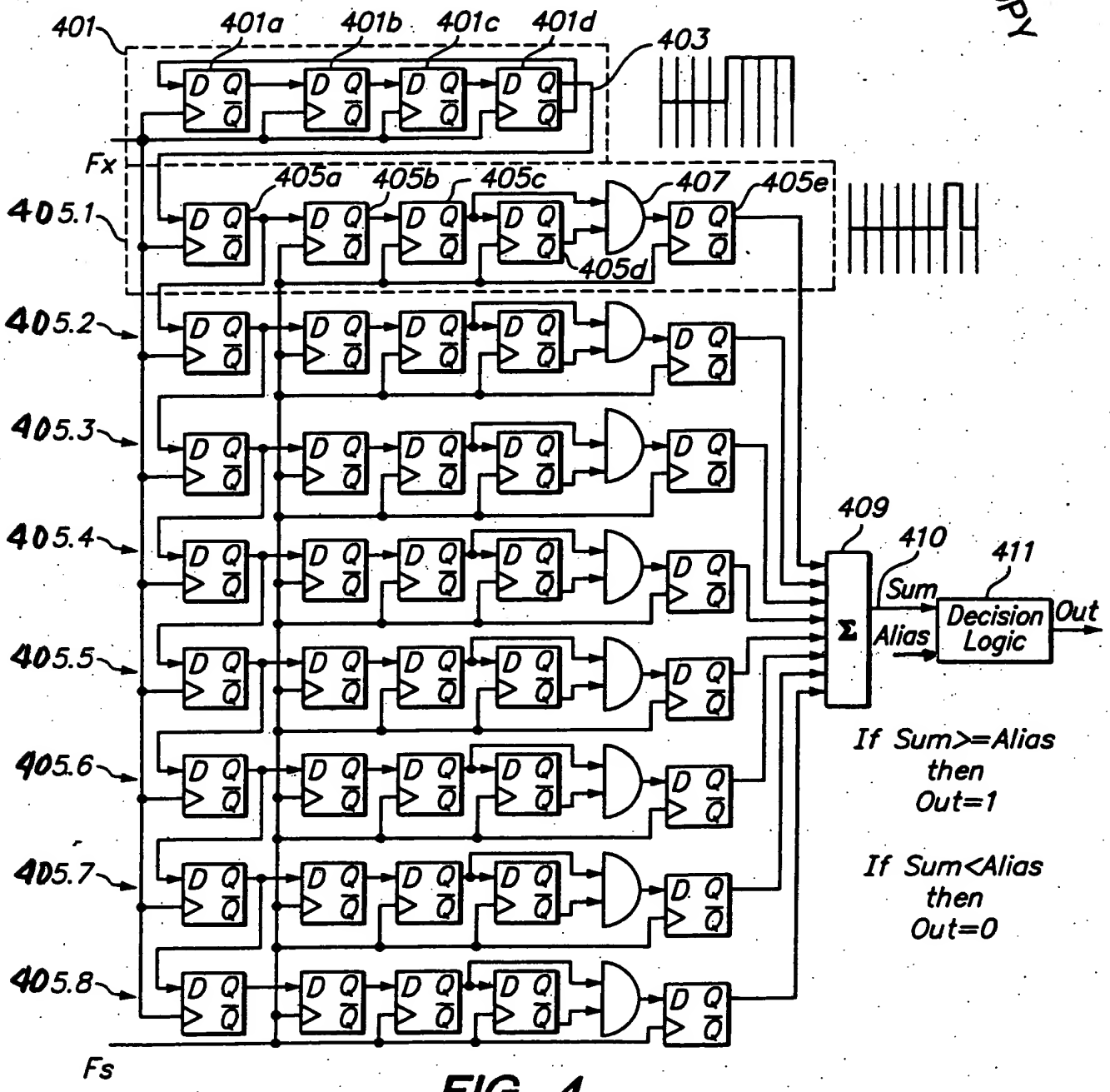

FIG. 4